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IMPLEMENTATION OF ADDRESS GENERATOR FOR WiMAX DEINTERLEAVER ON FPGA

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ABSTRACT
In this paper, a low-complexity and novel technique is proposed to implement the address generation circuitry of 2-D deinterleaver used in the WiMAX transreceiver using the Xilinx field-programmable gate array (FPGA). The floor function is associated with the implementation of the steps,that are required for the permutations of the incoming bit stream in channel interleaver/deinterleaver for IEEE 802.16e standard, it is very difficult to implement in FPGA. In this paper, we develop a simple algorithm along with its mathematical background and eliminates the requirement of floor function and allows low-complexity FPGA implementation. The use of the internal multiplier of FPGA and the sharing of resources for 16-quadrature-amplitude modulation (QAM),64-QAM and quadrature phase-shift keying modulations along with all possible code rates makes our approach to be novel and efficient when compared with conventional look-up table-based approach. The proposed approach yields significant improvement in the use of FPGA resources.

KEYWORDS: Deinterleaver/Interleaver circuits, Modulation Circuits, Wireless Systems.

INTRODUCTION
BROADBAND wireless access (BWA) is continuously becoming a more challenging competitor to the conventional wired last mile access technologies . IEEE has developed standards for mobile BWA (IEEE 802.16e) popularly referred to as mobile WiMAX. The channel interleaver employed in the WiMAX transreceiver plays a vital role in minimizing the effect of burst error. In this brief, a novel, low-complexity,high-speed, and resource-efficient address generator for the channel deinterleaver used in the WiMAX transreceiver eliminating the requirement of floor function is proposed.
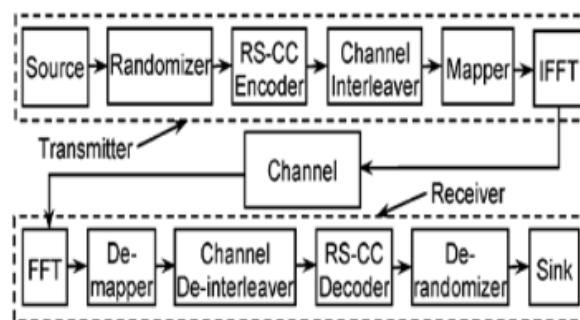
Fig:1 Block diagram of the WiMAX transreceiver.

The mandatory blocks of a WiMAX transreceiver are shown in Fig. 1. Data stream received from a source is randomized before being encoded by two forward error correction (FEC) coding techniques, namely, Reed– Solomon (RS) and convolutional coding (CC). The channel interleaver permutes the encoded bit stream to reduce the effect of burst error. When convolutional turbo code (CTC) is used for FEC, being optional in WiMAX, the channel interleaver

is not required, since CTC itself includes an interleaver within it.Modulation and construction of orthogonal frequency-division multiplexing symbols are performed by the two subsequent blocks, namely, mapper and inverse fast Fourier transform of Fig. 1. In the receiver, the blocks are organized in the reverse order enabling the restoration of the original data sequence at the output.
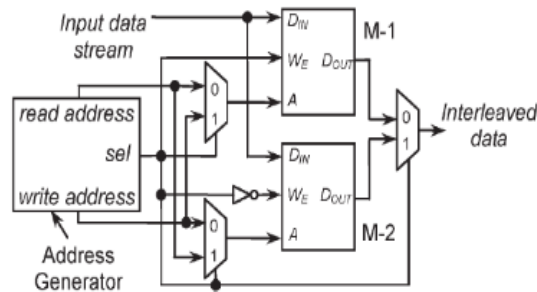

Fig:2Block diagram of interleaver/deinterleaver structure

Two-dimensional block inter leaver/deinterleaver structure,which is used as a channel interleaver/deinterleaver in the WiMAX system, is described in Fig. 2.Hardware Structure for Address Generator for WiMAX Using Different modulation techniques.

WI MAX TRANSRECEIVER SYSTEM
Now let us know about how the working principle carried out in WiMAX system. As we can see the mandatory blocks used in fig 1,the incoming data streams obtained from the source part is been encoded using two main Forward Error Correction (FEC) coding techniques and before this, randomization of data streams procedure will be carried out. By this process, effect of burst error is minimized using the permutation technique to the received data stream. Actually there is no need of channel interleaver part when Convolutional Turbo Code (CTC) is used. Because the interleaver part is inbuilt in CTC itself. Now when we look into the basic block diagram as shown in fig 1, there the mapper and inverse Fast Fourier Transform (FFT) block is used in order for modulation and construction of Orthogonal Frequency–Division Multiplexing (OFDM) process. Now in order to obtain the original data sequence at the output part, reverse order of restoration is been done.

When we look into fig 2 as shown, we can observe the read and write operation done in the address generator block. Since any one operation that is either read or write will be enable once at a time, we make use of multiplexer with select lines as shown. Observe that not gate is used in order to switch from one to the other operation. Here we can see that two memory blocks are used one for read and one for write operation where whenever the select line=1, Write enabled signal M-1 will be active and vice versa. Finally the interleaved data will be obtained as the output as seen by fig 2.
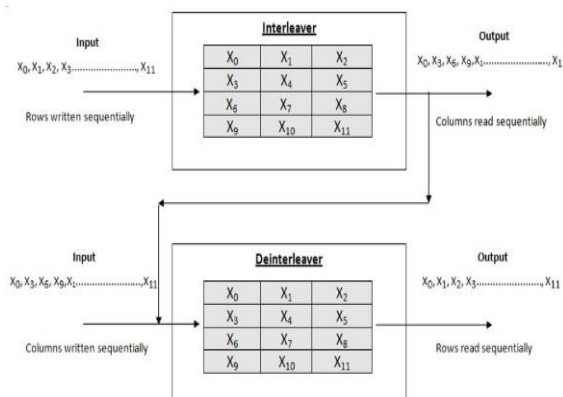

Fig 3: This is exactly how the block interleaver works

In block interleaver shown in fig 3, input symbols are written sequentially row by row and the output symbols are obtained by reading the column sequentially until the interleaver is emptied. While the interleaver is emptied, it is loaded again and the cycle repeats. At the receiver before decoding, the received bits are deinterleaved to get the original encoded data. This is in the form of M*N array where N is length of the code word.

INTERLEAVING IN WiMAX SYSTEM

The block interleaver/deinterleaver exploits different depths Ncbps to incorporate various code rates and modulation schemes (see Table I) for IEEE 802.16e. The data stream received from the RS-CC encoder is permuted by using the two-step processes described by (1) and (2). These steps ensure mapping of coded bits onto nonadjacent subcarriers and alternate less/more significant bits of the modulation constellation, respectively. Thus,

$$mk=(Ncbps/d).(k\%d)+[k/d] \qquad (1)$$
$$jk=s.[mk/s]+(mk+Ncbps–[d.mk/Ncbps])\%s \qquad (2)$$

$$m_j=s.[j/s]+(j+[d.j/Ncbps])\%s \qquad (3)$$

$$k_j=d.mj-(Ncbps-1).[d.mj/Ncbps] \qquad (4)$$

ALGORITHM FOR DEINTERLEAVER

ere, the proposed algorithm for address generator of the WiMAX deinterleaver along with its mathematical background has been described. Their direct implementation on an FPGA chip is not feasible. Table shows the deinterleaver addresses for the first four rows and five columns of each modulation type. As d =16 is chosen, the number of rows are fixed (= d) for all Ncbps, whereas the number of columns are given by Ncbps/d.
Table-1:Address generation of different schemes

DETERMINATION OF CORRELATION BETWEEN ADDRESSES

Row no.(j)	Column no. (i) →	0	1	2	3	4
0	N_{cbps} = 96-bits, ½ code rate, QPSK	d.0+0=0	d.1+0=16	d.2+0=32	d.3+0=48	d.4+0=64
1		d.0+1=1	d.1+1=17	d.2+1=33	d.3+1=49	d.4+1=65
2		d.0+2=2	d.1+2=18	d.2+2=34	d.3+2=50	d.4+2=66
3		d.0+3=3	d.1+3=19	d.2+3=35	d.3+3=51	d.4+3=67
0	N_{cbps} = 192-bits, ½ code rate, 16-QAM	d.0+0=0	d.1+0=16	d.2+0=32	d.3+0=48	d.4+0=64
1		d.1+1=17	d.0+1=1	d.3+1=49	d.2+1=33	d.5+1=81
2		d.0+2=2	d.1+2=18	d.2+2=34	d.3+2=50	d.4+2=66
3		d.1+3=19	d.0+3=3	d.3+3=51	d.2+3=35	d.5+3=83
0	N_{cbps} = 576-bits, ¾ code rate, 64-QAM	d.0+0=0	d.1+0=16	d.2+0=32	d.3+0=48	d.4+0=64
1		d.1+1=17	d.2+1=33	d.0+1=1	d.4+1=65	d.5+1=81
2		d.2+2=34	d.0+2=2	d.1+2=18	d.5+2=82	d.3+2=50
3		d.0+3=3	d.1+3=19	d.2+3=35	d.3+3=51	d.4+3=67

A close examination of the addresses in Table reveals that the correlation between them. The mathematical foundation of the correlation between the addresses, as derived in this brief.

$$k_{n,\text{QPSK}} = \{ d*i+j \quad \text{for } \forall j \text{ and } \forall i \tag{5}$$

$$k_{n,\text{16-QAM}} = \begin{cases} d*i+j & \text{for } j\%2 = 0 \text{ and for } \forall i \\ d*(i+1)+j & \text{for } j\%2 = 1 \text{ and} \\ & \text{for } i\%2 = 0 \\ d*(i-1)+j & \text{for } j\%2 = 1 \text{ and} \\ & \text{for } i\%2 = 1 \end{cases} \tag{6}$$

$$k_{n,\text{64-QAM}} = \begin{cases} d*i+j & \text{for } j\%3 = 0 \text{ and for } \forall i \\ d*(i-2)+j & \text{for } j\%3 = 1 \text{ and} \\ & \text{for } i\%3 = 2 \\ d*(i+1)+j & \text{for } j\%3 = 1 \text{ and} \\ & \text{for } i\%3 \neq 2 \\ d*(i+2)+j & \text{for } j\%3 = 2 \text{ and} \\ & \text{for } i\%3 = 0 \\ d*(i-1)+j & \text{for } j\%3 = 2 \text{ and} \\ & \text{for } i\%3 \neq 0 \end{cases} \tag{7}$$

Where $j = 0, 1, \ldots, d-1$ and $i = 0, 1, \ldots, (Ncbps/d)-1$ represent the row and column numbers, respectively, inTable-1[5]. In addition, kn represents the deinterleaver addresses. General validity of (5)–(7) to represent the correlation between addresses of Table has formally been proven using the algebraic analysis , which lacks the involvement of(5)–(7). The outcome of this analysis using (5)–(7) provides the same result, as shown in Table. Thus, (5)–(7) play the pivotal role in establishing formal mathe matical foundation of our proposed algorithm.

PROPOSED MODEL
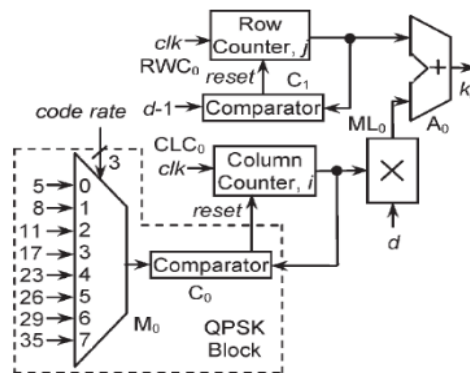
Fig:4a The address generator for QPSK

In order to test the proposed algorithms for the address generator of the WiMAX deinterleaver with all modulation schemes, transformation of these algorithms into digital circuits are made and are shown in Fig. 4(a)–(c). The QPSK hardware shown in Fig. 4(a) has a row counter RWC0 to generate row numbers between 0 and $d-1$. A column counter CLC0 with multiplexer M0 and comparator C0 generate the variable column numbers to implement permissible Ncbps. A multiplier ML0 and an adder A0 perform the desired operations to implement (5). The address generator for 16-QAM follows a similar structure, such as that of QPSK with few additional modules. These modules are designed with an incrementer, a decrementer, two modulo-2 blocks, and two multiplexers, as shown in Fig. 4(b). As per in the 64-QAMmodulation scheme, the address generator has to implement three different progressive patterns for the column numbers. The design procedure used in 16-QAM is extended in 64-QAM to meet this requirement with the use of additional hardware[6] and is shown in Fig. 4(c). A simple up counter generates the read addresses for the 2-D deinterleaver.
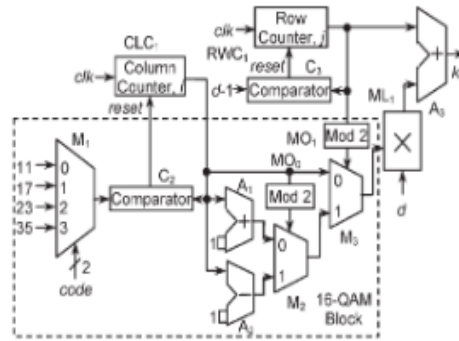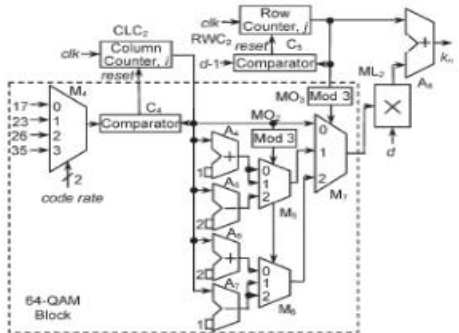
Fig:4bThe address generator for 16-QAM

Fig:4cThe address generator for 64-QAM

The top-level structure of the deinterleaver address generator is shown in Fig. 5. Logic circuits shown inside the dashed line in Fig. 4(a)–(c) are presented here as QPSK block, 16-QAM block, and 64-QAM block, respectively. Our design is optimized in the sense that common logic circuits such as multiplier, adder, row counter, and column counter are shared while generating addresses for any modulation type. In addition,the design also shares the incrementer and the decrementer required in 16-QAM and 64-QAM blocks.
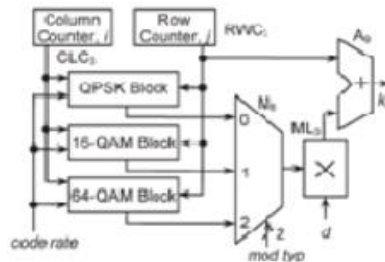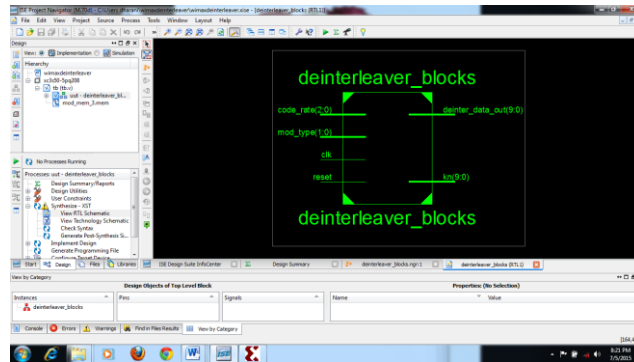

Fig 5:Top-level view of complete deinterleaver address generator.
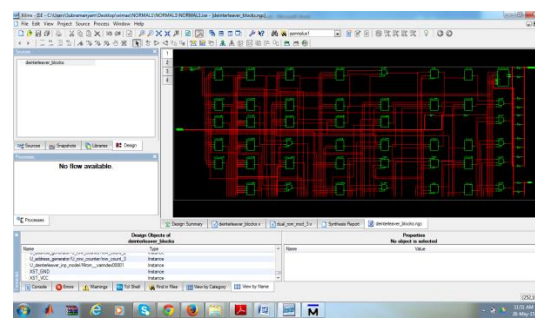
SIMULATION RESULTS
Below figures are schematic diagrams for deinterleaver /interleaver

RTL SCHEMATIC:
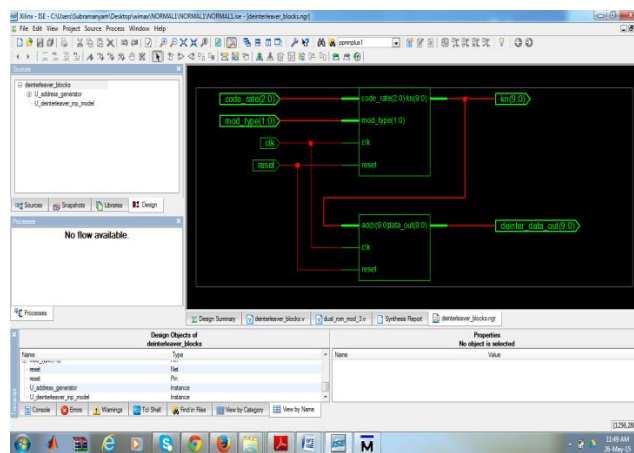
Fig: 6,7 RTL schematic for deinterleaver/interleaver

TECHNOLOGY SCHEMATIC:

Fig:8 Technology scematic for deinterleaver/interleaver

Simulation results are obtained fig 6-8 using Xilinx Isim for all permissible modulation types and code rates.Results are shown for selected data rate of each modulation type as shown below.
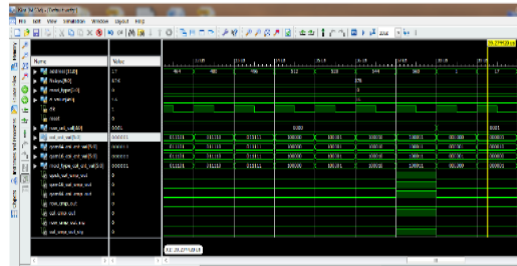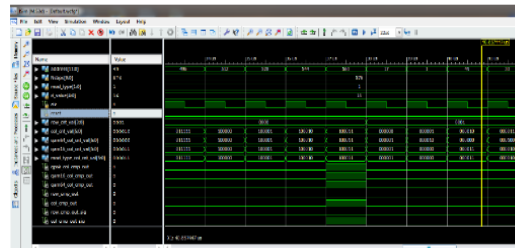
Fig 6: QPSK with Ncbps=576
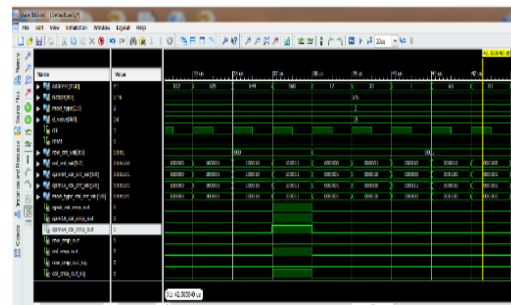

Fig 7: 16-QAM with Ncbps=576

Fig 8: 64-QAM with Ncbps=576

CONCLUSIONS

In this novel algorithm along with its mathematical formulation, including proof for address generation circuitry of the WiMAX channel deinterleaver supporting all possible code rates and modulation patterns as per IEEE802.16e. The proposed algorithm is converted into an optimized digital hardware circuit. The hardware is implemented on the Xilinx FPGA using Verilog HDL. Comparison of our proposed work with a conventional LUT-based method and also with a recent work show significant improvement on resource utilization and operating frequency.

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